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ANEBDNEBT IN THE CLAIMS:

1. (currently amended) A method of validating design of complex integrated circuits (IC) where a design process is carried out under electronic design automation (EDA) environment, comprising the following steps of:

building prototype silicon based on IC design data produced under the EDA environment;

applying event based test vectors derived from the IC design data to the prototype silicon by an event based test system and evaluating the response output of the prototype silicon, where the event based test vectors are test vectors in an event format in which an event is any change in a signal which is described by its timing and the event based test system is a test system for testing an IC by utilizing the event based test vectors;

modifying the event based test vectors by the event based test system to acquire desired response outputs from the silicon prototype; and

feedbacking the modified event based test vectors to the EDA environment to modify the IC design data, thereby correcting design errors in the IC design data.

2. (original) A method of validating design of complex integrated circuits as defined in Claim 1, further comprising a step of linking EDA tools including a simulator with the event based test system through a software interface.

3. (original) A method of validating design of complex integrated circuits as defined in Claim 1, further comprising a step of extracting event format data through a testbench produced in the IC design data.

4. (currently amended) A method of validating design of complex integrated circuits as defined in Claim 3, wherein said step of extracting the event format data ~~**including**~~ includes a step of executing the testbench by the simulator and extracting the event format data from a value change dump file produced by the simulator.

5. (currently amended) A method of validating design of complex integrated circuits as defined in Claim 3, further comprising a step of installing the extracted event data in the event based test system and generating event based test vectors using the extracted event data by the event based test system to apply the test vectors to the prototype silicon.

6. (original) A method of validating design of complex integrated circuits as defined in Claim 1, further comprising a step of creating a new testbench based on the modified event based test vectors from the event based test system.

7. (currently amended) A method of validating design of complex integrated circuits as defined in ~~**Claim 1**~~ Claim 2, wherein said EDA tools ~~**including**~~ includes means for viewing and editing waveforms derived from the testbench created in the IC design data.

8. (currently amended) A method of validating design of complex integrated circuits as defined in Claim 1, wherein said event based test system ~~including~~ includes means for viewing and editing waveforms of event based test vectors extracted from a testbench created in the IC design data and means for changing clock ~~rate~~ rates and event timing data of the event based test vectors applied to the prototype silicon.

9. (currently amended) A method of validating design of complex integrated circuits (IC) where a design process is carried out under electronic design automation (EDA) environment, comprising the following steps of:

building prototype silicon based on IC design data produced under the EDA environment;

linking EDA tools including a simulator with an event based test system;

extracting event format data from ~~data~~ a value change dump file resulted from executing a testbench produced in the IC design data by the simulator;

installing the extracted event data in the event based test system and generating event based test vectors using the event data by the event based test system;

applying the event based test vectors to the prototype silicon and evaluating the response output of the prototype silicon, where the event based test vectors are test vectors in an event format in which an event is any change in a signal

which is described by its timing and the event based test system is a test system for testing an IC by utilizing the event based test vectors;

modifying the event based test vectors by the event based test system to acquire desired response outputs from the silicon prototype; and

feedbacking the modified event based test vectors to the EDA tools to modify the design data, thereby correcting design errors in the design data;

whereby validating the design of the IC without conducting an in-system test of the silicon prototype.

10. (currently amended) A method of validating design of complex integrated circuits (IC) where a design process is carried out under electronic design automation (EDA) environment, comprising the following steps of:

preparing a device model of an IC to be designed based on IC design data produced under the EDA environment;

applying event based test vectors derived from the IC design data to the device model by an event based test system and evaluating the response output of the device model, where the event based test vectors are test vectors in an event format in which an event is any change in a signal which is described by its timing and the event based test system is a test system for testing an IC by utilizing the event based test vectors;

modifying the event based test vectors by the event based test system to acquire desired response outputs from the device model; and

feedbacking the modified event based test vectors to the EDA environment to modify the IC design data, thereby correcting design errors in the IC design data.

11. (original) A method of validating design of complex integrated circuits as defined in Claim 10, wherein said device model is either dependent of a particular simulator or independent of any simulator.

12. (original) A method of validating design of complex integrated circuits as defined in Claim 10, further comprising a step of linking EDA tools including a simulator with the event based test system through a software interface.

13. (original) A method of validating design of complex integrated circuits as defined in Claim 10, further comprising a step of extracting event format data through a testbench produced in the IC design data.

14. (currently amended) A method of validating design of complex integrated circuits as defined in Claim 13, wherein said step of extracting the event format data ~~**including**~~ includes a step of executing the testbench by the simulator and extracting the event format data from ~~a~~ the value change dump file produced by the simulator.

15. (currently amended) A method of validating design of complex integrated circuits as defined in Claim 13, further comprising a step of installing the extracted event data in the event based test system and generating event based test vectors using the extracted event data by the event based test system to apply the event based test vectors to the device model.

16. (original) A method of validating design of complex integrated circuits as defined in Claim 10, further comprising a step of creating a new testbench based on the modified event based test vectors from the event based test system.

17. (currently amended) A method of validating design of complex integrated circuits as defined in Claim ~~10~~ 12, wherein said EDA tools ~~including~~ includes means for viewing and editing waveforms derived from the testbench created in the IC design data.

18. (currently amended) A method of validating design of complex integrated circuits as defined in Claim 10, wherein said event based test system ~~including~~ includes means for viewing and editing waveforms of event based test vectors extracted from a testbench created in the IC design data and means for changing clock ~~rate~~ rates and event timing data of the event based test vectors applied to the device model.

19. (currently amended) A method of validating design of complex integrated circuits (IC) where a design process is carried out under electronic design automation (EDA) environment, comprising the following steps of:

preparing a device model of an IC to be designed based on IC design data produced under the EDA environment;

linking EDA tools including a simulator with an event based test system;

extracting event format data from ~~**data**~~ a value change dump file resulted from executing a testbench produced in the IC design data by the simulator;

installing the extracted event data in the event test system and generating event based test vectors using the event data by the event based test system;

applying the event based test vectors to the device model and evaluating the response output of the device model, where the event based test vectors are test vectors in an event format in which an event is any change in a signal which is described by its timing and the event based test system is a test system for testing an IC by utilizing the event based test vectors;

modifying the event based test vectors by the event test system to acquire desired response outputs from the device model; and

feedbacking the modified event based test vectors to the EDA tools to modify the design data, thereby correcting design errors in the design data.